In the Claims:

1. (Currently Amended) A mixer circuit comprising:

a gain stage coupled to receive a first signal on a first input and a modulated bias current on a common node, and in accordance therewith, produce an output signal, the gain stage having a first current;

a current shunt circuit coupled between the common node and a reference voltage, the current shunt circuit ~~having~~ providing a second current from the reference voltage to the common node, wherein the first current and the second current are coupled to the common node; and

a bias circuit to generate the modulated bias current, the bias circuit having an input coupled to receive a second signal, and in accordance therewith, generate the modulated bias current, and an output coupled to the common node to provide the modulated bias current to the gain stage.

2. (Original) The mixer circuit of claim 1 wherein the second current controls the gain of the gain stage and bias circuit.

3. (Currently Amended) The mixer circuit of claim 1 wherein the current shunt circuit comprises a MOS transistor having a gate terminal, a source terminal, and a drain terminal, one of the source terminal and the drain terminal coupled ~~between~~ to the common node and the other of the source terminal and the drain terminal coupled to the reference voltage.

4. (Original) The mixer circuit of claim 3 wherein the reference voltage is a supply voltage.

5. (Original) The mixer circuit of claim 3 wherein current shunt circuit further comprises a resistor coupled in series between the common node and the MOS transistor.

6. (Original) The mixer circuit of claim 1 wherein the second signal is an RF signal and the first signal is a differential signal.

7. (Original) The mixer circuit of claim 6 wherein the frequency of the differential signal is an integer fraction of the frequency of the RF signal.

8. (Original) The mixer circuit of claim 7 wherein the integer fraction is one-third.

9. (Original) The mixer circuit of claim 6 wherein the differential signal is approximately a square wave.

10. (Original) The mixer circuit of claim 6 wherein the differential signal is generated by a local oscillator, and wherein the output of the local oscillator is amplified to generate a differential signal that approximates a square wave.

11. (Original) The mixer circuit of claim 1 wherein the bias circuit comprises a first transistor having a control input and a first and second output, wherein the control input is coupled to receive an RF signal, the first output is coupled to a second reference voltage, and the second output is coupled to the common node.

12. (Original) The mixer circuit of claim 11 wherein the first transistor is an NMOS transistor.

13. (Original) The mixer circuit of claim 11 wherein the bias circuit further comprises a capacitor having a first terminal coupled to the gate of the first transistor and a second terminal coupled to receive the RF input signal.

14. (Original) The mixer circuit of claim 1 wherein the gain stage is a differential stage and the first signal is a differential signal.

15. (Original) The mixer circuit of claim 14 wherein the differential stage comprises:

a first transistor having a control input and first and second outputs, the control input coupled to receive a first component of the differential signal;

a second transistor having a control input and first and second outputs, the control input coupled to receive a second component of the differential signal; and

a load coupled to the first output of the first transistor and to the first output of the second transistor, wherein the second output of the first transistor and the second output of the second transistor are coupled together and to the common node.

16. (Original) The mixer circuit of claim 15 wherein the first and second transistors are NMOS transistors.

17. (Original) The mixer circuit of claim 15 wherein the load comprises a first resistor coupled between the first output of the first transistor and a supply voltage and a second resistor coupled between the first output of the second transistor and the supply voltage.

18. (Original) The mixer circuit of claim 1 wherein the reference voltage is a supply voltage.

19. (Withdrawn) A receiver circuit comprising:

an input amplifier coupled to receive an input radio frequency (RF) signal; and

a mixer circuit having a first input coupled to an output of the input amplifier and a second input coupled to receive a differential oscillating signal, the mixer circuit comprising:

a gain stage configured to receive a first signal and a modulated bias current, and in accordance therewith, produce an output signal, the gain stage generating a first current and receiving the modulated bias current on a common node;

a current shunt circuit coupled between the common node and a reference voltage, the current shunt circuit configured to generate a second current, wherein the first current and the second current are coupled to the common node; and

a bias circuit to generate the modulated bias current, the bias circuit having an input configured to receive a second signal, and in accordance therewith, generate the modulated bias current, and an output coupled to the common node to provide the modulated bias current to the gain stage.

20. (Withdrawn) The receiver of claim 19 further comprising a low pass filter coupled to the output of the mixer.

21. (Withdrawn) The receiver of claim 20 further comprising a automatic gain control block coupled to the output of the low pass filter.

22. (Withdrawn) The receiver of claim 19 further comprising a voltage controlled oscillator coupled to the differential input mixer circuit.

23. (Withdrawn) A transceiver comprising a receiver circuit of claim 19 coupled to a transmitter circuit.

24. (Withdrawn) An electronic system comprising a transceiver of claim 23 coupled to an interface bus, the electronic system being capable of wireless data communications with another electronic system via the transceiver.

25. (Withdrawn) The electronic system of claim 24 wherein the electronic system is a personal computer.

26. (Withdrawn) The electronic system of claim 25 wherein the personal computer further comprises a central processing unit (CPU), a memory, and I/O devices coupled to the interface bus.

27. (Currently Amended) A method of mixing signals in a mixer circuit comprising:

generating a first current in a differential stage;

generating a second current in a shunt circuit coupled between the common node and a reference voltage, the second current provided from the reference voltage to the common node;

coupling the first current and the second current through a common node to generate a bias current in a bias circuit;

receiving an RF signal in the bias circuit;

receiving a second signal in the differential stage; and

generating a mixer output in accordance with the RF signal and the second signal.

28. (Original) The method of claim 27 further comprising modulating the bias current in accordance with the RF signal.

29. (Original) The method of claim 27 further comprising coupling the modulated bias current into the differential stage through the common node.

30. (Original) The method of claim 27 wherein the frequency of the second signal is an integer fraction of the frequency of the RF signal.

31. (Original) The method of claim 30 wherein the integer fraction is one-third.

32. (Original) The method of claim 27 wherein the mixer output is proportional to the product of the first signal and the second signal.

33. (Withdrawn) A method of mixing signals in a mixer comprising: biasing a gain stage of the mixer using a first current having a first magnitude at a first frequency of operation; and biasing the gain stage of the mixer using a second current having a second magnitude at a second frequency of operation.

34. (Withdrawn) The method of claim 33 wherein the first current is less than the second current, and wherein the first frequency is lower than the second frequency.

35. (Withdrawn) The method of claim 33 further comprising shunting a portion of the first current to a reference voltage.

36. (Withdrawn) The method of claim 35 wherein a first portion of the first current is shunted to the reference voltage at low frequencies, and second portion, less than the first portion, is shunted to the reference voltage at high frequencies.

37. (Withdrawn) The method of claim 36 wherein the second portion is substantially zero.

38. (Withdrawn) The method of claim 36 wherein the second portion is shunted through an inductor.